IN THE CLAIMS:

1-23 (Canceled)

24. (Currently Amended) A method for selecting nodes in a electronic circuit to be optimized, comprising:

examining each node according to a minimum path slack and a maximum path slack associated with the node; and

putting nodes into a plurality of criticality bins according to the minimum path slacks and maximum path slacks associated with the nodes, wherein each criticality bin ~~stores nodes with~~ is defined by a ~~corresponding~~ range of minimum path slacks ~~and~~ or a ~~corresponding~~ range of maximum path slacks.

25. (Original) The method of claim 24, wherein said plurality of criticality bins comprises:

a first criticality bin for nodes with critical minimum path slacks and non-critical maximum path slacks;

a second criticality bin for nodes with sub-critical minimum path slacks and non-critical maximum path slacks;

a third criticality bin for nodes with critical minimum path slacks and sub-critical maximum path slacks;

a fourth criticality bin for nodes with sub-critical minimum paths slacks and sub-critical maximum path slacks;

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a fifth criticality bin for nodes with critical minimum path slacks and critical maximum path slacks; and

a sixth criticality bin for nodes with sub-critical minimum path slacks and critical maximum path slacks.

26. (Original) The method of claim 25, wherein:

said critical minimum path slacks include minimum path slacks less than a first minimum slack;

said sub-critical minimum path slacks include minimum path slacks greater than said first minimum slack and less than a second minimum slack;

said non-critical minimum path slacks include minimum path slacks greater than said second minimum slack;

said critical maximum path slacks include maximum path slacks less than a first maximum slack;

said sub-critical maximum path slacks include maximum path slacks greater than said first maximum slack and less than a second maximum slack; and

said non-critical maximum path slacks include maximum slacks greater than said second maximum slack.

27. (Currently Amended) The method of claim 26, wherein:

the first minimum slack is 0;

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the second minimum slack is 100 picoseconds;

the first maximum slack is 0; and

the second ~~minimum~~ maximum slack is 100 picoseconds.

28. (Original) The method of claim 24, further comprising:

selecting a criticality bin from said plurality of criticality bins; and

putting nodes in said selected criticality bin into a number of a plurality of slack bins divided between a first minimum path slack and a second minimum path slack.

29. (Original) The method of claim 28, wherein the first minimum path slack is the most negative minimum path slack of the nodes in said criticality bin and the second minimum path slack is 0.

30. (Currently Amended) The method of claim 28, further comprising:

putting nodes into a plurality of level bins, wherein each level bin is defined by ~~comprises~~ a range of node levels ~~and~~ in timing paths;

selecting a slack bin from said plurality of slack bins; and

putting nodes in said selected slack bin into a said plurality of level bins according to their associated node levels in timing paths.

31. (Original) The method of claim 30, further comprising:

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selecting a node; and

optimizing said node to remove a timing violation.

32. (Original) The method of claim 31, wherein said optimizing said node comprises:

determining a required delay between a driver and a receiver;

selecting a buffer to be inserted between said driver and said receiver;

determining an input transition time to said buffer from said driver;

determining a desired effective load on said buffer that causes said buffer to generate said required delay under said input transition time;

determining a desired effective length of a wire that generates said desired effective load;

determining a length of a conductor between said driver and said receiver inside a bounding box that encloses said driver and said receiver;

determining a maximum effective load generated by said length of a conductor, if said desired effective load is less than or equal to said maximum effective load, inserting said buffer at a point inside said bounding box; and

if said desired effective load is greater than said maximum effective load, inserting said buffer at a point outside said bounding box.

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33. (Original) The method of claim 31, further comprising:

performing an incremental analysis to re-determine minimum and maximum path slacks of nodes affected by said optimization; and

again putting said nodes in said plurality of level bins according to their node levels in timing paths.

34. (Currently Amended) The method of claim 33, further comprising:

reducing said ~~the~~ number of a plurality of slack bins by one;

again putting said nodes into said plurality of slack bins.

35. (Original) The method of claim 34, further comprising again putting said nodes in said plurality of criticality bins.

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